AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Previously presented) A method of managing power consumption in a computing system having a plurality of performance states, including a maximum performance state and a plurality of other performance states that provide successively less performance capability for an integrated circuit, the method comprising:

determining utilization of the integrated circuit; and

each time the computing system determines that a higher performance state is required based on the determined utilization while in each of the other performance states, changing to a predetermined performance state, skipping all intermediate performance states between a current performance state and the predetermined performance state.

2. (Previously presented) The method as recited in claim 1 wherein the predetermined performance state is the maximum performance state.

3. (Original) The method as recited in claim 1 wherein the predetermined performance state is a near maximum performance state.

4. (Previously presented) The method as recited in claim 1 further comprising:

comparing the determined utilization to a threshold utilization value to determine if a higher performance state is required;

comparing the integrated circuit utilization to a second threshold utilization value; and

if the integrated circuit utilization is below the second threshold utilization value, always entering a next lower performance state as a next performance state.

5. (Previously presented) The method as recited in claim 1 further comprising:

comparing the determined utilization to a threshold utilization value to determine if a higher performance state is required;

comparing the integrated circuit utilization to a second threshold utilization value;

if the integrated circuit utilization is below the second threshold utilization value,

entering a lower performance state as a next performance state, the lower performance state being determined according to integrated circuit utilization.

6. (Original) The method as recited in claim 4 wherein the performance state is lowered by reducing at least one of the voltage and frequency.

7. (Original) The method as recited in claim 1 wherein the performance state is reduced by reducing both voltage and clock frequency of the integrated circuit.

8. (Original) The method as recited in claim 1 wherein determining the utilization is done periodically.

9. (Original) The method as recited in claim 1 wherein the integrated circuit includes a central processing unit.

10. - 18. (Canceled)

19. (Previously presented) A computing system comprising:

an integrated circuit having multiple performance states;

means for determining utilization of the integrated circuit; and

means for changing, while in each of the performance states other than a maximum performance state, from a current performance state to the maximum performance state, skipping all intermediate performance states between the current performance state and the maximum performance state, each time the computing system determines that a higher performance is required based on the determined utilization.

20. (Canceled)

21. (Original) The computing system as recited in claim 19 further comprising:

means for determining that the utilization is below a second threshold value and for always changing operation of the integrated circuit from the current performance state to a next lowest performance state in response to a determination that the utilization is below a second threshold utilization value.

22. (Original) The computing system as recited in claim 19 further comprising:

means for determining that the utilization is below a second threshold value and for changing operation of the integrated circuit from the current performance state to a lower performance state in response to a determination that the utilization is below a second threshold utilization value, the lower performance state being determined according to the integrated circuit utilization.

23. - 32. (Canceled)